REMARKS

Claims 1-4 and 7-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamiya, *et al.* (U. S. Patent No. 6,080,624) taken with the Applicant's admitted prior art (AAPA). Claims 1-4, 6-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA taken with Kamiya, *et al.* Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya, *et al.* and the AAPA, and further in view of Ma, *et al* (U.S. Patent No. 5,280,446) or Fazan, *et al* (U.S. Patent No. 6,066,528). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The present invention of amended claims 1-6 is directed to a method of fabricating a NAND-type flash memory device. A plurality of isolation layers running parallel with each other are formed at predetermined regions of a semiconductor substrate. A string selection line pattern, a plurality of word line patterns and a ground selection line pattern are formed crossing over the isolation layers and active regions between the isolation layers. Impurities are ion-implanted into the active regions among the string selection line pattern, the word line patterns and the ground selection line pattern. Drain regions are formed at the active regions adjacent to the string selection line pattern and opposite the ground selection line pattern. Source regions are also formed at the active regions adjacent to the ground selection line pattern and opposite the string selection line pattern. A first interlayer insulating layer is formed on the entire surface of the substrate including the drain and source regions. The first interlayer insulating layer is patterned to form a slit-type common source line contact hole exposing the source regions and the isolation layers between the source regions. A common source line is formed filling the common source line contact hole such that a top surface level of the common source line is even with or lower than a top surface level of the first interlayer insulating layer.

The present invention of amended claims 7-12 further includes forming drain contact holes exposing respective drain regions and forming drain contact plugs filling respective drain contact holes.

The claims are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the top surface level of the common source line is even with or lower than a top surface level of the first interlayer insulating layer. With reference to Figures 7A and 7B, it can be seen that, in the present invention, a top surface level of the common source line is even with or lower than a top surface level of the first interlayer insulating layer. That is, a top surface level of the common source line 48 is substantially even with a top surface level of the first interlayer insulating layer 41 (see page 13, line 22 through page 14, line 5 of the present specification). This feature prevents a protrusion due to the common source line 48 from being formed on the fist interlayer insulating layer 41 and thereby the aspect ratio of the bit line contact hole and the operation speed of the NAND-type flash memory device are improved (see page 16, lines 11 through16 of the present specification).

It is believed that this subject matter, now set forth in the amended claims, is neither taught nor suggested by any of the cited prior art, taken alone or in combination.

Kamiya, *et al.* is directed to a NOR type flash EEPROM in which source contact holes 130a, and drain contact holes 130b are formed in a matrix between two layered gates 118 on the substrate 111, as shown in Figure 9B. Specifically, the interlayer insulation film 130 is etched to open the upper portion of the drain diffusion layers 120b of the cell transistors in the column direction and also to open the upper portions of the source diffusion layers 120a of the cell transistors 101 arranged in the row direction, as shown in Figures 10 and 11. As a result, the parts of the etched interlayer insulation film for contact holes 130a and 130b are completely removed and the tungsten film 151 is filled in the etched part, as shown in Figure 11. Contact holes 130a and 130b, which are arranged in the matrix, are formed by etching the tungsten film 151 (see Figures 4-12 and column 6,

line 63 through column 8, line23). The resultant contact holes 130a and 130b are formed between two layered gate sections 118 without remaining interlayer insulation film 130 between contact holes 130a, 130b and the two layered gate sections 118, as shown in Figures 12 and 14.

Kamiya, *et al.* fail to teach or suggest forming a common source line filling the common source line contact hole, wherein a top surface level of the common source line is even with or lower than a top surface level of the first insulating layer, as claimed in the amended claims.

In Kamiya, *et al.* contact holes 130a and 130b, which may be considered analogous to the common source line of the present invention, are formed between two layered gate sections 118 without any remaining interlayer insulation film 130, which may be considered analogous to the first interlayer insulation layer of the present invention, between contact holes 130a, 130b and the two layered gate sections 118. Thus, a top surface level of contact holes 130a, 130b is neither even with nor lower than a top surface level of the first insulating layer and is only even with the two layered gate sections 118, because the interlayer insulation film 130 is all eliminated in the contact hole portion.

The AAPA also fails to teach or suggest this subject matter now set forth in the amended claims. In the AAPA, a top surface level of common source line 5 is higher than a top surface level of first interlayer insulating layer 4 and the common source line is interposed between the first and second interlayer insulating layers 4 and 6, as shown in Figure 2B. In this configuration, the common source line is interposed between the first and second interlayer insulating layers 4, 6. The thickness of the common source line and the thickness of the second interlayer insulating layer should be increased, which cause the aspect ratio of the bit line contact holes and the resistance of the common source line to be increased (see page 2, line 7 through page 3, line 21). In accordance with the invention, to overcome these limitations of AAPA, the common source line is formed such that a top surface level of the common source line is even with or lower than a top surface level of the first interlayer insulating layer. This is in contrast with the common source line of the

AAPA.

Since neither of Kamiya, *et al.* and the AAPA teach or suggest the invention set forth in the amended claims, there is no combination of the references that would provide such teaching or suggestion. That is, there is no combination of the references which would result in teaching or suggesting forming a common source line filling a common source line contact hole, wherein a top surface level of the common source line is even with or lower than a top surface level of a first interlayer insulating layer, as claimed in the amended claims. Accordingly, it is believed that the amended claims are allowable over the cited references. Therefore, reconsideration of the rejections of claims 1-4 and 7-10 under 35 U.S.C. § 103(a) based on Kamiya, *et al.* taken with the AAPA and the rejections of claims 1-4, 6-10 and 12 under 35 U.S.C. § 103(a) based on the AAPA taken with Kamiya, *et al.* is respectfully requested.

Neither of the Ma, *et al.* and Fazan, *et al.* references teaches or suggests forming a common source line filling a common source line contact hole, wherein a top surface level of the common source line is even with or lower than a top surface level of a first interlayer insulating layer, as set forth in the amended claims. Accordingly, there is no combination of Kamiya, *et al.*, the AAPA, Ma, *et al.* and Fazan, *et al.* which would result in providing such teaching or suggestion. Accordingly, it is believed that the amended claims are allowable over all four references, and reconsideration on the rejections of claims 5 and 11 under 35 U.S.C. § 103(a) based on Kamiya, et al, the AAPA and Ma, *et al.* or Fazan, *et al.* is respectfully requested.

In view of the amendments made to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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